TITLE

METHOD FOR DESIGNING DE-EMPHASIS CIRCUIT FOR VIDEO SIGNAL PROCESSING INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT MADE BY THE SAME

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from my application *DE-EMPHASIS CIRCUIT DESIGN METHOD OF VIDEO SIGNAL PROCESSING IC AND IC USING THEREOF* filed with the Korean Industrial Property Office on 5 September 2000 and there duly assigned Serial No. 52372/2000.

BACKGROUND OF THE INVENTION

Technical Field

[0002] The present invention relates to a video signal processing integrated circuit (IC) and an IC designing method and, more particularly, to a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and to an IC made by the method.

Related Art

[0003] A typical video cassette recorder (VCR) playback circuit includes a video head 110, a

rotary transformer, a pre-amplifier, and a video signal processing IC. In the playback (PB) mode, a modulated video signal is detected by the video head, is input to the pre-amplifier via the rotary transformer for amplification with a predetermined gain, and is then input to the video signal processing IC which blocks a low-frequency component color signal among the signals input thereto and allows a frequency-modulated (FM) luminance signal having a high-frequency component to pass through. The high-pass filtered FM luminance signal is demodulated, and the demodulated luminance signal is subject to high-frequency component noise reduction and is then applied to a de-emphasis unit.

[0004] The de-emphasis unit compensates the demodulated luminance signal so that it has a frequency characteristic of the luminance signal before recording. The PB video level varies according to a gain which is set during manufacture of the video signal processing IC. Since the gain is set by means of a resistor having a certain value, an error in the PB level may be generated in the actual manufacturing process depending on deviation in the value of the resistor.

[0005] As described above, the video signal processing IC is designed such that a variable resistor or fixed resistor is necessarily added to the de-emphasis output pin port of the video signal processing IC. This increases the number of components, thereby lowering the manufacturing efficiency, increasing the cost of the product, and causing a deviation in the PB level due to resistance variation of the fixed resistor on the exterior of the IC.

SUMMARY OF THE INVENTION

[0006] To solve the above problems, it is an object of the present invention to provide a de-

emphasis circuit designing method for a video signal processing integrated circuit (IC) in order to minimize the number of peripheral components of the video signal processing IC by incorporating a circuit device for determining the level of a reproduced video signal of the de-emphasis circuit, and to an IC made by the latter method.

[0007] Accordingly, to achieve the above object, there is provided a method for designing a video signal processing IC incorporating a luminance signal processing block and a color signal processing block having a de-emphasis circuit. A circuit element for determining the level of a reproduced video signal of the de-emphasis circuit is incorporated into the video signal processing IC, and the circuit element is connected to a ground exclusively used for luminance signal processing.

[0008] According to another aspect of the present invention, there is provided a video signal processing IC incorporating a circuit for determining the level of a reproduced video signal of a de-emphasis circuit having a reproduced video level setting unit. The reproduced video level setting unit includes an amplification unit for amplifying a demodulated luminance signal output from the de-emphasis circuit, and a gain-controlled switching unit connected to a plurality of resistance elements for determining the gain of the amplification unit, for switching electrical connection of the plurality of resistance elements according to the reproduced video level during manufacture of the video signal processing IC, and for determining the gain of the amplification unit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, and wherein:

[0010] Fig. 1 is a schematic diagram illustrating a reproducing circuit of a video cassette recorder (VCR) having a video signal processing IC;

[0011] Fig. 2 is a schematic diagram illustrating a reproducing circuit of a video cassette recorder (VCR) having a video signal processing IC according to the present invention;

[0012] Fig. 3 is a diagram illustrating the relationship between modulation/demodulation of a frequency modulated (FM) signal and a video signal; and

[0013] Fig. 4 is a detailed circuit diagram illustrating the PB level setting unit shown in Fig. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0014] This invention will now be described in more detail with reference to the drawings, in which Fig. 1 is a schematic diagram illustrating a reproducing circuit of a video cassette recorder (VCR) having a video signal processing IC.

[0015] As shown in Fig. 1, a video cassette recorder (VCR) playback circuit includes a video head 110, a rotary transformer 120, a pre-amplifier 130, and a video signal processing integrated circuit (IC) 140 comprising a high-pass filter (HPF) 141, a limiter 142, a demodulator 143, a low-pass filter (LPF) 144, a de-emphasis unit 145, a playback (PB) level setting unit 146 and a mixer

147.

[0016] In the PB mode, a modulated video signal detected by the video head 110 is input to the pre-amplifier 130 via the rotary transformer 120 for amplification with a predetermined gain by the pre-amplifier 130, and is then input to the HPF 141 of the video signal processing IC 140.

[0017] The HPF 141 blocks a low-frequency component color signal among the signals input thereto, and allows a frequency-modulated (FM) luminance signal having a high-frequency component to pass through. The high-pass filtered FM luminance signal passes through the limiter 142, which prevents black-and-white inversion occurring during demodulation, and is then demodulated in the demodulator 143. The demodulated luminance signal is then input to the LPF 144, which reduces high-frequency component noise, and the output of LPF 144 is then applied to the de-emphasis unit 145.

[0018] The de-emphasis unit 145 is designed to have a frequency characteristic inversely symmetrical with respect to that of pre-emphasis in the recording mode. Accordingly, the de-emphasis unit 145 functions to compensate the demodulated luminance signal so that it has a frequency characteristic of the luminance signal before recording. The PB video level varies according to the gain of an amplifier is the de-emphasis unit 145. The gain of the PB level setting unit 146 is determined during manufacture of the video signal processing IC 140. That is, during manufacture of the video signal processing IC 140, the gain of the PB level setting unit 146 is set in accordance with a resistance of resistor R1 attached to pin P1. Thus, an error in the PB level may be generated in the actual manufacturing process depending on variation in the resistance of the resistor R1.

[0019] The luminance signal output from the de-emphasis unit 145 is mixed with a color signal output from a color signal playback processing procedure by the mixer 147, and is then output to pin P2.

[0020] As described above, the video signal processing IC is designed such that a variable resistor or fixed resistor for determining gain is necessarily added to the de-emphasis output pin port of the video signal processing IC. This increases the number of components, thereby lowering manufacturing efficiency, increasing the cost of the product, and causing a deviation or variation in the PB level due to a resistance variation of the fixed resistor on the exterior of the IC.

[0021] Fig. 2 is a schematic diagram illustrating a reproducing circuit of a video cassette recorder (VCR) having a video signal processing IC according to the present invention.

[0022] As shown in Fig. 2, a reproducing circuit for a VCR having a video signal processing IC according to the present invention includes a video head 210, a rotary transformer 220, a pre-amplifier 230, and a video signal processing IC 240 having a high-pass filter (HPF) 241, a limiter 242, a demodulator 243, a low-pass filter (LPF) 244, a de-emphasis unit 245, a playback (PB) level setting unit 246, and a mixer 247.

[0023] In general, the de-emphasis unit 245 and the PB level setting unit 246 are incorporated into a single de-emphasis circuit, and are thus processed in a single circuit block.

[0024] The detailed circuitry of the PB level setting unit 246 is shown in Fig. 4, as discussed below.

[0025] First, the basic operation of the VCR will be described. During a reproduction mode, a

modulated video signal detected by video head 210 is input to the pre-amplifier 230 via the rotary transformer 220, and is amplified with a predetermined gain in the pre-amplifier 230 for output to the HPF 241 of the video signal processing IC 240.

[0026] The HPF 241 blocks low-frequency color signal components contained in the modulated video signal, and produces an FM luminance signal having a high-frequency component.

[0027] The FM luminance signal output from the HPF 241 is a mixed signal comprising a low-frequency FM wave having a large amplitude and a high-frequency FM carrier wave having a low amplitude. Signal components are easily volatile at a low-amplitude area of a high-frequency portion of the FM wave, resulting in black-and-white inversion during demodulation. In order to prevent the black-and-white inversion, the high-pass filtered FM luminance signal is limited to a constant reference level by the limiter 242.

[0028] The demodulator 243 receives the output of the limiter 242, and demodulates the same to restore the FM luminance signal having a frequency deviation of 1 MHz into an unmodulated state signal. Then, the demodulated luminance signal is noise-attenuated by the LPF 244 for input to the de-emphasis unit 245.

[0029] The de-emphasis unit 245 includes an internal amplifier circuit which has a frequency characteristic inversely symmetrical with respect to pre-emphasis before modulation. The signal from LPF 244 has its gain adjusted by the de-emphasis unit 245 so as to adapt the output level of a reproduced video signal to a prescribed level, and that adjustment is performed by the PB level setting unit 246.

[0030] The reproduced video signal is defined so as to have a level of 1 Vpp by demodulating an FM video signal having a frequency deviation of 1 MHz in accordance with the Video Home System (VHS) standard, as shown in Fig. 3, which is a diagram illustrating the relationship between modulation/demodulation of a frequency modulated (FM) signal and a video signal. However, the slope of the linear relationship between the reproduced luminance signal level and a frequency deviation during demodulation may decrease or increase, as indicated by dotted arrow *a* or *c*, due to a difference or variation in the characteristics of circuit elements caused during the process of manufacturing the video signal processing IC 240. Accordingly, in the course of manufacturing the video signal processing IC 240, the PB level setting unit 256 controls so that the reproduced luminance signal level is accurately set to 1 Vpp with respect to the frequency deviation of 1 MHz in a graphical representation of the relationship between the reproduced luminance signal level and the frequency deviation during demodulation.

[0031] The operation of the PB level setting unit 246 will now be described with reference to Fig. 4, which is a detailed circuit diagram illustrating the PB level setting unit shown in Fig. 2.

[0032] The output signal of the de-emphasis unit 245 is applied to a base terminal of the transistor Q1. The circuit formed by the transistor Q1 and resistors R0, R1,..., Rn is an amplification unit. The gain of the amplification unit is determined by the value of the resistors R1, R2,..., Rn which are parallel-connected to a collector terminal of the transistor Q1.

[0033] The resistors R1, R2,..., Rn are grounded through switches SW1, SW2,..., SWn, respectively. Thus, the resistors connected to those of the switches SW1, SW2,..., SWn which are in the OFF state do not affect the gain value, and only the resistors connected to switches in

the ON state affect the gain value of the amplification unit. In particular, the ground to which the switches SW1, SW2,..., SWn are connected is a ground used exclusively for luminance signal processing, and is different from the ground used for color signal reproduction processing. This feature (separation of the grounds used for luminance signal processing and color signal processing, respectively) is for the purpose of preventing noise generated in the course of processing a color signal from affecting the luminance signal.

[0034] The FM luminance signal having a frequency deviation of 1 MHz is input to the demodulator 243 of the video signal processing IC 240 of Fig. 2 during manufacture of the video signal processing IC 240 using the above-described principle. Then, the gain level of the amplification unit constituting the PB level setting unit 246 is determined such that the reproduced video signal level output from the video signal processing IC 240 becomes 1 Vpp under a termination condition of 75 Ω. Then, ON/OFF switching of the switches SW1, SW2,..., SWn of the gain-controlled switching unit 10 of Fig. 4 is carried out, depending on the determined gain, to determine the resistance value of the collector terminal of the transistor Q1.

[0035] The switches SW1, SW2,..., SWn constituting the gain-controlled switching unit 10 are, preferably, constructed using Zener diodes, and can be designed so as to determine ON/OFF switching using Zener breakdown characteristics of the Zener diodes. In other words, if a voltage greater than a breakdown voltage is applied to a Zener diode so that it is switched on, a Zener breakdown phenomenon, in which the resistance of the Zener diode becomes substantially zero, occurs and the Zener diode is shorted (this is generally called "Zener Zapping").

[0036] As described above, according to the present invention, all circuit elements constituting

a circuit which determines the level of a reproduced video signal of de-emphasis circuit 245 are incorporated into video signal processing IC 240 at the time of design of the video signal processing IC 240, thereby removing external circuit elements, including a resistor at the output terminal of the de-emphasis circuit 245 of the video signal processing IC 240.

[0037] In the embodiment of the present invention, the amplification unit in the PB level setting unit 246 is designed using a single transistor Q1 and resistors R1, R2, R3, ..., Rn. There may be a case in which the amplification unit is designed using a differential amplifier.

[0038] According to the embodiment of the present invention, the number of components can be reduced by designing all circuit elements constituting a circuit which determines the level of a reproduced video signal of de-emphasis circuit 245 so as to be incorporated into a video signal processing IC 240 at the time of design of the video signal processing IC 240, thereby reducing cost. Also, deviation in the PB level due to external component deviation can be reduced. Further, the material cost can also be reduced.

[0039] It should be understood that the present invention is not limited to the particular embodiment disclosed herein as the best mode contemplated for carrying out the present invention, but rather that the present invention is not limited to the specific embodiments described in this specification except as defined in the appended claims.